CLAIMS

Having thus described the invention, what is claimed is:

1. A method, comprising:

placing a memory structure in a path of a JTAG scan chain in response to an instruction, the memory structure having multiple locations, at least portions of the memory structure being capable of storing first data and second data;

serially receiving at least one signal containing first data via the JTAG scan chain;

storing the first data in the memory structure;

receiving at least one other signal from at least one component on the JTAG scan chain;

transmitting the other signal to at least one other component on the scan chain;

placing second data into the memory structure; and

serially transmitting the second data via the JTAG scan chain.

2. The method of claim 1, wherein the component is selected from the group consisting of at least one of multiple devices on a JTAG scan chain, and an emulator.

3. The method of claim 1, wherein said second data comprises information responsive to the other signal.

4. The method of claim 3, wherein the other signal comprises a non-JTAG signal.

5. The method of claim 3, wherein said receiving comprises receiving the other signal from an emulator.

6. The method of claim 5, wherein:

the other signal comprises a reset signal, and is transmitted to a plurality of devices on the scan chain.

7. The method of claim 3, wherein said receiving comprises receiving the other signal from a device on the scan chain.

8. The method of claim 7, wherein the other signal comprises a reset signal.

9. The method of claim 7, wherein said transmitting comprises transmitting the other signal to a plurality of other devices on the scan chain.

10. The method of claim 7, wherein said receiving comprises receiving other signals from multiple devices on the JTAG scan chain.

11. The method of claim 10, wherein said receiving comprises receiving other signals from each of the multiple devices.

12. The method of claim 10, wherein said receiving is effected via parallel connections to each of the multiple devices.

13. The method of claim 1, wherein said placing a memory structure comprises serially receiving the instruction from an emulator coupled to the scan chain.

14. The method of claim 1, wherein said serially transmitting comprises transmitting the second data to an emulator coupled to the JTAG scan chain.

15. The method of claim 1, wherein said transmitting comprises transmitting the other signal to at least one device on the scan chain via at least one parallel connection.

16. The method of claim 15, wherein said transmitting comprises transmitting the other signal to each device on the scan chain via multiple parallel connections.

17. The method of claim 1, wherein the other signal comprises an interrupt signal.

18. The method of claim 1, further comprising:

placing second memory structures of multiple devices on the scan chain;

coupling a third memory structure to the scan chain in parallel with the second memory structures;

the third memory structure having at least as many locations as a combination of the second memory structures.

19. The method of claim 18, wherein the second memory structures comprise Instruction Registers.

20. The method of claim 18, wherein the second memory structures comprise Idcode registers.

21. The method of claim 18, further comprising coupling a Bypass register to the third memory structure.

22. The method of claim 21, comprising actuating the Bypass register upon receipt of a Bypass instruction in the third memory structure.

23. The method of claim 1, wherein the instruction comprises a JTAG compliant Controller Select instruction.

24. The method of claim 1, wherein the first data is selected from the group consisting of Reset Enable, Test Reset Enable, Interrupt Enable, JTAG Break Enable for Processor, JTAG Break Enable from another Controller, Clear, and combinations thereof.

25. The method of claim 1, wherein the second data is selected from the group consisting of Reset Occurred, Reset Logic Level, Interrupt Occurred, JTAG Break Occurred by Processor, JTAG Break Occurred from another Controller, and combinations thereof.

26. A controller for controlling multiple components, comprising:

an instruction memory structure;

a data memory structure;

control logic coupled to the instruction memory structure and the data memory structure;

signal logic coupled to the data memory structure;

a JTAG-compliant TAP controller coupled to the instruction memory structure;

a serial input port;

a serial output port;

at least one of said serial input port and said serial output port being selectively couplable to at least one of the instruction memory structure and the data memory structure;

a plurality of parallel inputs coupled to the signal logic and available to receive signals from each of the multiple components;

a plurality of parallel outputs coupled to the signal logic and available to transmit signals to each of the multiple components;

the control logic being configured to couple the data memory structure to the serial input port and serial output port upon implementation of an instruction in the instruction memory structure;

the signal logic being configured to receive and transmit signals between the multiple components upon receipt via the serial input port of first data in a first location of the data memory structure;

the signal logic being configured to place second data into a second location of the data memory structure in response to said first data; and

the data memory structure being configured to serially transmit the first and second data via the serial output port.

27. The controller of claim 26, wherein at least one of said serial input port and said serial output port are selectively couplable to at least one of an instruction register a bypass register, and an idcode register.

28. The controller of claim 26, wherein the multiple components include multiple devices and a JTAG connector coupled to the scan chain.

29. The controller of claim 28, wherein the multiple devices comprise three devices.

30. The controller of claim 26, wherein the devices are soft cores implemented in at least one computer readable medium.

31. The controller of claim 30, wherein the devices are implemented in an FPGA.

32. The controller of claim 26, being implemented in a computer readable medium, and wherein the devices are soft cores disposed in said computer readable medium.

33. The controller of claim 32, wherein said computer readable medium comprises an FPGA.

34. The controller of claim 32, being configured to enable the soft cores to be loaded into said computer readable medium via the scan chain.

35. The controller of claim 26, configured for being responsive to JTAG and non-JTAG signals.

36. The controller of claim 26, wherein the components are selected from the group consisting of at least one of multiple devices on a JTAG scan chain, and an emulator.

37. The controller of claim 26, wherein said second data comprises information responsive to the other signal.

38. The controller of claim 37, wherein the signals comprises non-JTAG signals.

39. The controller of claim 37, wherein the signal logic is configured to receive a signal from an emulator.

40. The controller of claim 39, wherein:

the signal comprises a reset signal, and the signal logic is configured to transmit the reset signal to a plurality of devices on the scan chain.

41. The controller of claim 26, wherein a signal is received from a device on the scan chain.

42. The controller of claim 41, wherein the signal comprises a reset signal.

43. The controller of claim 41, wherein the signal is transmitted to a plurality of other devices on the scan chain.

44. The controller of claim 41, wherein other signals are received from multiple devices on the JTAG scan chain.

45. The controller of claim 44, wherein other signals are received from each of the multiple devices.

46. The controller of claim 26, being configured to serially receive the instruction from an emulator coupled to the scan chain.

47. The controller of claim 26, being configured to transmit the second data to an emulator coupled to the JTAG scan chain.

48. The controller of claim 26, being configured to transmit a signal to at least one device on the scan chain via at least one parallel connection.

49. The controller of claim 48, being configured to transmit a signal to each device on the scan chain via multiple parallel connections.

50. The controller of claim 26, wherein the signal comprises an interrupt signal.

51. The controller of claim 26, further comprising:

a second memory structure configured for being disposed on the scan chain in series with second memory structures of devices in the scan chain;

a third memory structure configured for being coupled to the scan chain in parallel with

each of the second memory structures;

the third memory structure having at least as many locations as a combination of each of the second memory structures.

52. The controller of claim 51, wherein the second memory structures comprise Instruction Registers.

53. The controller of claim 51, wherein the second memory structures comprise Idcode registers.

54. The controller of claim 51, further comprising a Bypass register coupled to the third memory structure.

55. The controller of claim 54, wherein the Bypass register is actuatable upon receipt of a Bypass instruction in the third memory structure.

56. The controller of claim 26, wherein the instruction comprises a JTAG compliant Controller Select instruction.

57. The controller of claim 26, wherein the first data is selected from the group consisting of Reset Enable, Test Reset Enable, Interrupt Enable, JTAG Break Enable for Processor, JTAG Break Enable from another Controller, Clear, and combinations thereof.

58. The method of claim 26, wherein the second data is selected from the group consisting of Reset Occurred, Reset Logic Level, Interrupt Occurred, JTAG Break Occurred by Processor, JTAG Break Occurred from another Controller, and combinations thereof.

59. A method comprising:

transmitting a first instruction to place multiple instruction memory structures on a JTAG scan chain;

serially transmitting a second instruction via the JTAG scan chain, the second instruction

to place a controller data memory structure on the JTAG scan chain;

serially transmitting at least one signal containing first controller data via the JTAG scan chain;

transmitting at least one other signal to a component on the JTAG scan chain; and

serially receiving second controller data corresponding to multiple devices from the data memory structure via the JTAG scan chain.

60. The method of claim 59, further comprising re-transmitting the first instruction after said serially receiving.

61. The method of claim 59, wherein said second controller data comprises information responsive to the other signal.

62. The method of claim 61, wherein the other signal comprises a non-JTAG signal.

63. The method of claim 61, wherein the other signal comprises a reset signal, and is transmitted to a plurality of devices on the scan chain.

64. The method of claim 59, wherein said second data indicates the other signal was transmitted to multiple devices on the JTAG scan chain.

65. The method of claim 59, wherein the other signal comprises an interrupt signal.

66. An emulator for debugging multiple devices on a JTAG scan chain, comprising:

a processor;

a scan chain signal handler configured to transmit and receive signals via the scan chain;

a TAP controller signal handler configured to send and receive instructions via parallel connections to each TAP controller on the scan chain; and

a non-JTAG signal handler configured to transfer non-JTAG signals to and from a controller disposed on the scan chain.

67. The emulator of claim 66, wherein:

said scan chain signal handler is configured to transmit a first instruction to place multiple instruction memory structures on a JTAG scan chain;

said TAP controller signal handler is configured to serially transmit a second instruction via the JTAG scan chain to place a controller data memory structure on the JTAG scan chain;

said scan chain signal handler being further configured to serially transmit at least one signal containing first controller data via the JTAG scan chain;

said non-JTAG signal handler being configured to transmit at least one other signal to at least one device on the JTAG scan chain; and

said scan chain signal handler being configured to serially receive second controller data corresponding to multiple devices from the data memory structure via the JTAG scan chain.

68. The emulator of claim 66, comprising:

a JTAG connector configured for coupling the emulator to the scan chain.

69. The emulator of claim 68, further comprising:

a controller coupled to said JTAG connector.

70. The emulator of claim 69, wherein said controller comprises:

a data memory structure;

control logic coupled to the instruction memory structure and the data memory structure;

signal logic coupled to the data memory structure;

a JTAG-compliant TAP controller coupled to the instruction memory structure;

a serial input port;

a serial output port;

at least one of said serial input port and said serial output port being selectively couplable to one of the instruction memory structure and the data memory structure;

a plurality of parallel inputs coupled to the signal logic and available to receive signals from each of the multiple components;

a plurality of parallel outputs coupled to the signal logic and available to transmit signals to each of the multiple components;

the control logic being configured to couple the data memory structure to the serial input port and serial output port upon implementation of an instruction in the instruction memory structure;

the signal logic being configured to receive and transmit signals between the multiple components upon receipt via the serial input port of first data in a first location of the data memory structure;

the signal logic being configured to place second data into a second location of the data memory structure in response to said first data; and

the data memory structure being configured to serially transmit the first and second data via the serial output port.

71. The emulator of claim 69, comprising:

a plurality of devices coupled to said controller in the scan chain.

72. The emulator of claim 71, wherein said controller and said devices comprise program code disposed on a computer readable medium.

73. The emulator of claim 72, wherein said computer readable medium comprises an FPGA.

74. A method, comprising:

with an emulator, transmitting a first instruction to place multiple instruction memory structures on a JTAG scan chain, the scan chain including a plurality of devices and a controller;

with the emulator, serially transmitting a second instruction via the JTAG scan chain;

placing a memory structure of the controller in a path of the JTAG scan chain in response to the second instruction, the memory structure having multiple locations, at least portions of the memory structure being capable of storing first data and second data;

with the emulator, serially transmitting at least one signal containing first controller data via the JTAG scan chain;

serially receiving the one signal with the controller;

storing the first data in the memory structure;

transmitting at least one other signal from the emulator;

receiving the other signal with the controller;

transmitting the other signal from the controller to the plurality of devices;

using the controller to place second data into the memory structure;

serially transmitting the second data corresponding to the devices via the JTAG scan chain; and

serially receiving the second data with the emulator via the JTAG scan chain.

75. A system comprising:

a JTAG scan chain including multiple devices;

an emulator for debugging the multiple devices, including:

a processor;

a scan chain signal handler coupled to the scan chain to transmit and receive signals;

a TAP controller signal handler configured to send and receive instructions via parallel connections to each TAP controller on the scan chain; and

a non-JTAG signal handler configured to transfer non-JTAG signals to and from a controller disposed on the scan chain; and

a controller, including:

an instruction memory structure;

a data memory structure;

control logic coupled to the instruction memory structure and the data memory structure;

signal logic coupled to the data memory structure;

a JTAG-compliant TAP controller coupled to the instruction memory structure;

a serial input port coupled to the scan chain signal handler;

a serial output port coupled to the scan chain;

at least one of said serial input port and said serial output port being selectively couplable to one of the instruction memory structure and the data memory structure;

a plurality of parallel inputs coupled to the signal logic and to each of the multiple components and to the non-JTAG signal handler;

a plurality of parallel outputs coupled to the signal logic and to each of the

multiple components and to the non-JTAG signal handler;

the control logic being configured to couple the data memory structure to the serial input port and serial output port upon implementation of an instruction in the instruction memory structure received from the emulator;

the signal logic being configured to receive and transmit signals between the multiple components upon receipt via the serial input port of first data in a first location of the data memory structure;

the signal logic being configured to place second data into a second location of the data memory structure in response to said first data; and

the data memory structure being configured to serially transmit the first and second data via the serial output port to the emulator.